A W-Band, High-Gain, Low-Noise Amplifier Using PHEMT MMIC

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***Abstract*—A W-band, high-gain, low-noise amplifier based on pseudomorphic InGaAs/GaAs HEMT devices has been developed. The amplifier has a measured about 50-dB stable gain, and 6-dB noise figure from 91 to 95 GHz. The overall amplifier measured 1.068″×1.281″×0.72″ and consumes a total dc power of 560 mW. These results demonstrate the highest gain ever achieved at these frequencies.**

I. Introduction

In the past, receiver performance at W-band has been dictated by the conversion loss (noise figure) of diode mixers. Recent advances in low-noise HEMT technology [1]–[5] show that the receiver noise figure can be improved by using a low-noise amplifier at the receiver front-end. In addition, these high-gain and low-noise amplifier at W-band also allow new system concepts to be applied. In this letter, we report about 50-dB gain performance from a 91–95-GHz amplifier with about 6-dB noise figure. This amplifier can be used in system applications such as low-noise receivers and radiometers. These results represent the highest gain ever achieved by a single amplifier at these frequencies.

II. Design Approach

Recent results show that typical HEMT amplifier has 6–7-dB small signal [1], [2] gain per stage at W-band. Therefore, eight (8) gain stages are necessary to produce 50 dB of gain. At such a high frequency, laborious tuning is unavoidable in a hybrid design using discrete devices because of the assembly and bondwire tolerance. While tuning a two- or three-stage amplifier has not been easy, tuning a eight-stage amplifier with 50-dB gain is formidable. On the other hand, mm-wave MMIC amplifiers are a challenge to provide a stable, high-gain design with a reasonable processing yield from a single chip.

Our approach to the 50-dB gain amplifier design is to use our two-stage MMIC PHEMT amplifiers [1] as the building block in a hybrid amplifier. A complete 50-dB amplifier consists of two waveguide-to-microstrip finline transitions, four MMIC chips and four interconnect edge coupled line on fused silica substrates as shown in Fig. 2.

The MMIC chips were mounted on carriers for characterization before final amplifier integration. To maximize the amplifier assembly yield, each MMIC chip could have been assembled on an individual carrier. However, this approach would have required the amplifier module to be integrated on four fixtures (carriers). Extra care in mechanical design, fabrication, and assembly would have been required to ensure good ground contacts between carriers. On the other hand, while mounting all four MMIC chips on a single carrier could

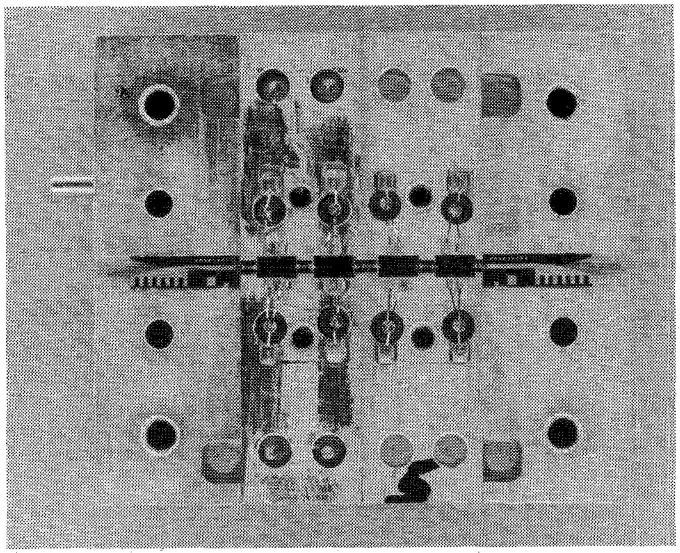

Fig. 1. Photograph of an assembled four-chip/eight-stage amplifier and waveguide to microstrip transitions.

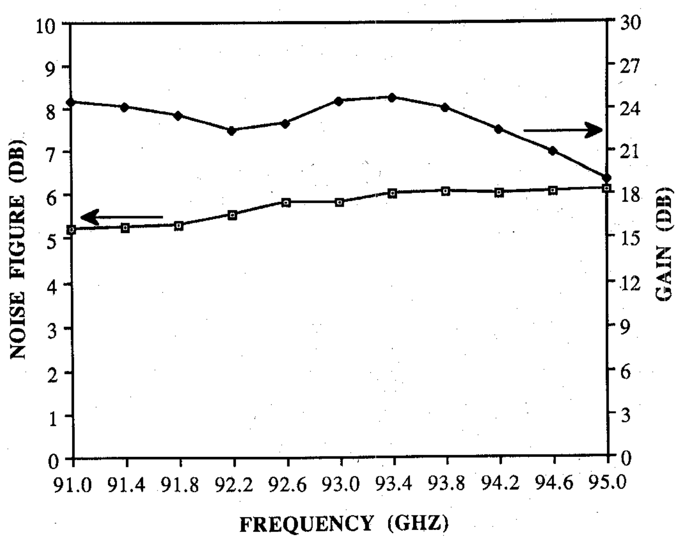

Fig. 2. Measured noise figure and associated gain of two MMIC chips (including finline transition loss).

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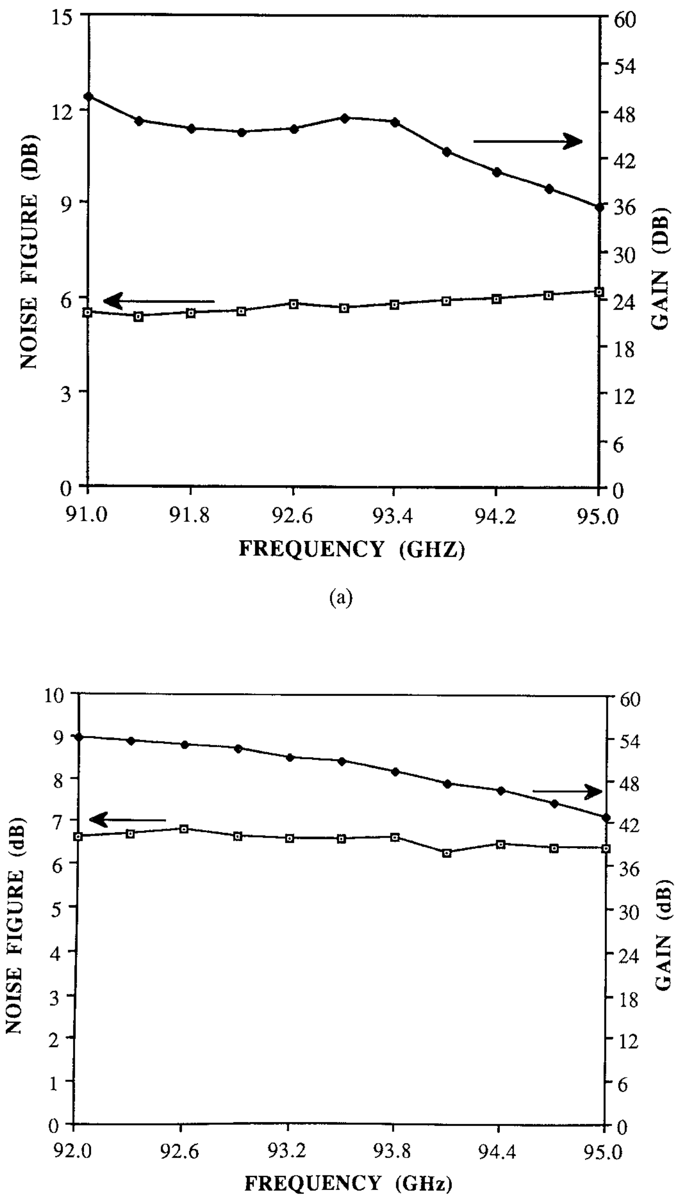
eliminate the concern over electrical contacts, it may result in a low assembly yield, because we have to discard the whole amplifier if any one chip fails to perform. As a compromise, we have selected a carrier that allows the cascading of two MMIC chips.

The carrier is designed to accommodate two MMIC chips and two coupled lines for dc blocking, To avoid problems related to waveguide moding, the carrier is channelized so that the circuit is operating below the cutoff frequency of the channel. In addition, to suppress the low-frequency oscillation, two capacitors (1 pF and 1000 pF) are integrated in both gate and drain bias circuits near the MMIC chips. During the course of amplifier development, we found that the assembly yield was almost 100% and no ground contact problems was observed.

III. Results

Each carrier was characterized before the final amplifier integration and is, in fact, a four-stage amplifier. The measurement was conducted using a waveguide noise figure/gain test set. Without any tuning, a typical performance of a two chip carrier is shown in Fig. 2, with 5-dB noise figure and 24-dB associated gain from 91–95 GHz, when biased for low-noise. This result is already the highest gain reported at W-band.

By integrating two carriers into one amplifier module, we have demonstrated the first eight-stage 50-dB high-gain amplifier at W-band. Fig. 3(a) shows the low-noise amplifier performance when biased for low noise, resulting in a noise figure of 5.5–6 dB with the associated gain of 40–49 dB from 91–95 GHz. Fig. 3(b) shows the low-noise amplifier performance when biased for high gain, giving a noise figure of 6.5–6.8 dB with the associated gain of 43–54 dB and from 92–95 GHz. The overall amplifier measured 1.068″ × 0.281″ × 0.72″ and consumes a total dc power of 560 mW. To achieve a stable amplifier with such a high gain at W-band, care was required to suppress moding feedback, through carrier design and incorporation of millimeter wave absorber within the amplifier housing. The final amplifier is completely stable at all bias conditions.



(b)

Fig. 3 Measured noise figure and associated gain of complete four-chip/eight-stage amplifier (including finline transition loss). (a) Biased for low noise. (b) Biased for high gain.

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